

*Fig. 1*

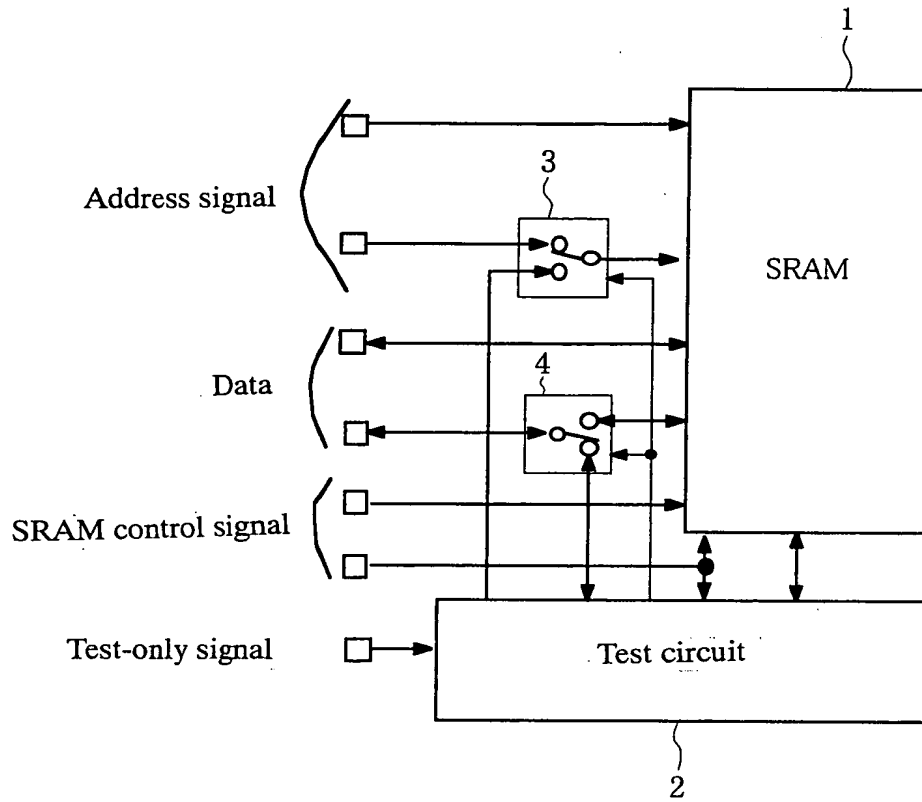


Fig. 2

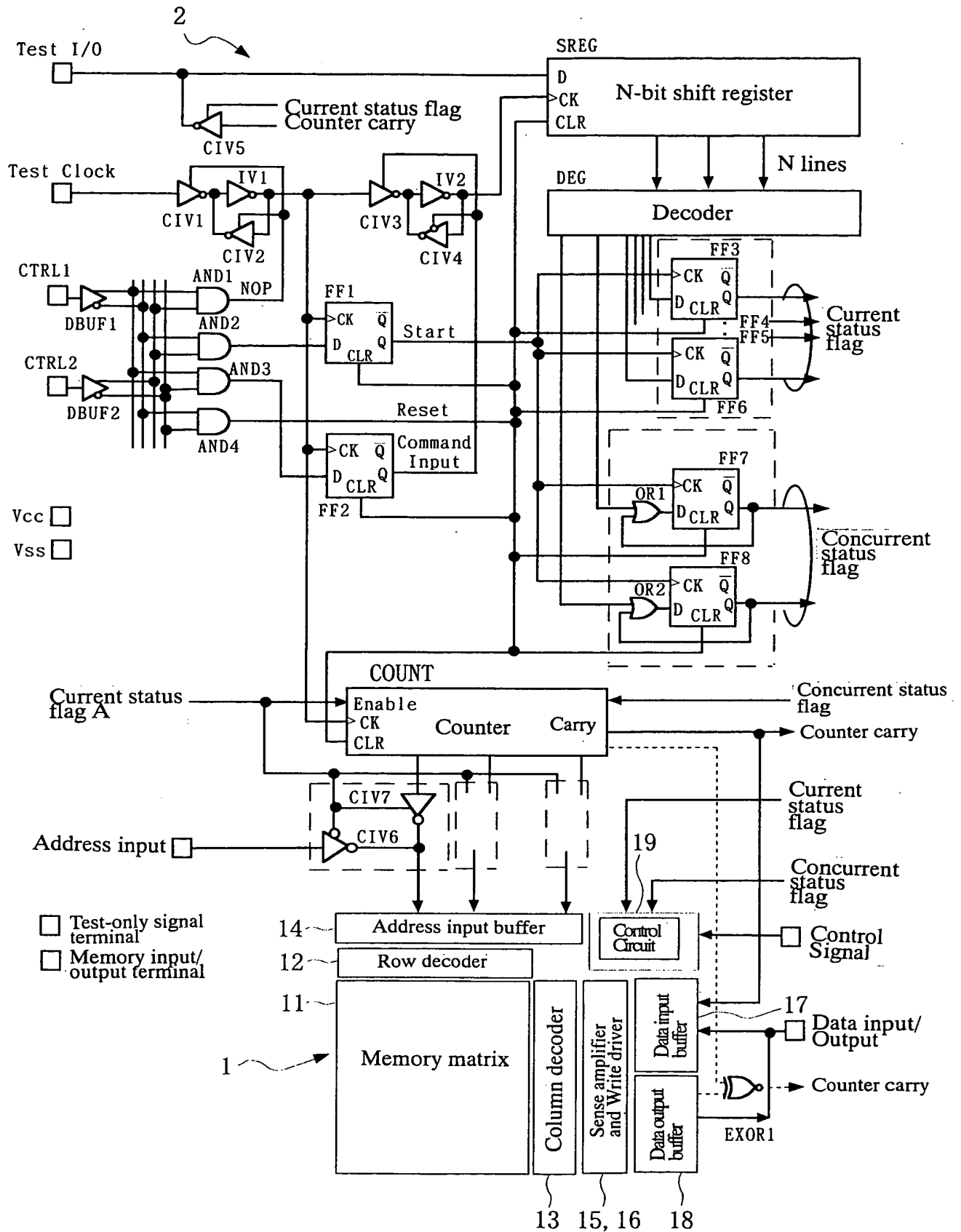


Fig. 3

Test Clock	CTRL1	CTRL2	Test I/O	Command register	Status
X	0	0	X	Reset to 000	Reset of test circuit, Deactivation of test circuit
L→H	0	1	X	Set of input command	Operational start of test circuit
L→H	1	0	Command input	Input of TEST I/O	Reception of test command
L→H	1	1	X	No change	NOP

Fig. 4

Test mode	Test command			Status of test circuit	Function of Test I/O at test mode
	1st·Cyc	2nd·Cyc	3rd·Cyc		
Current mode	0	0	0	Deactivation of test circuit	Memory data terminal
	0	0	1	Burn-in (Write) operation	Borrow output of address counter
	0	1	0	Burn-in (Read) operation	Borrow output of address counter
	0	1	1	Monitor burn-in operation	0: PASS 1: Fail output
Concurrent mode	1	0	0	Establishment of multi-choice mode flag	In conformity to current mode
	1	0	1	Establishment of redundant bit mode flag	
	1	1	0	Outside regulation	
	1	1	1	Outside regulation	

*Fig. 5*

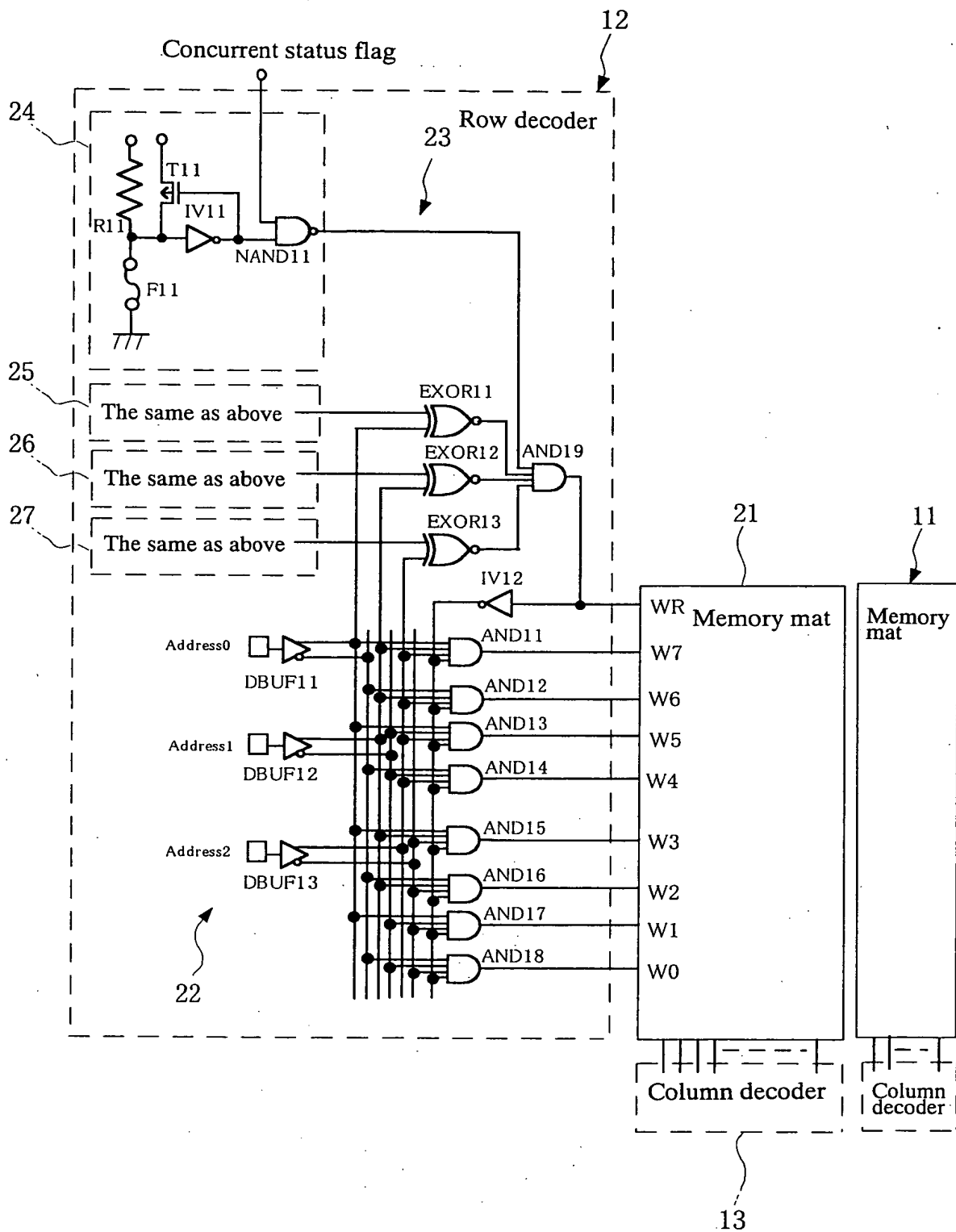
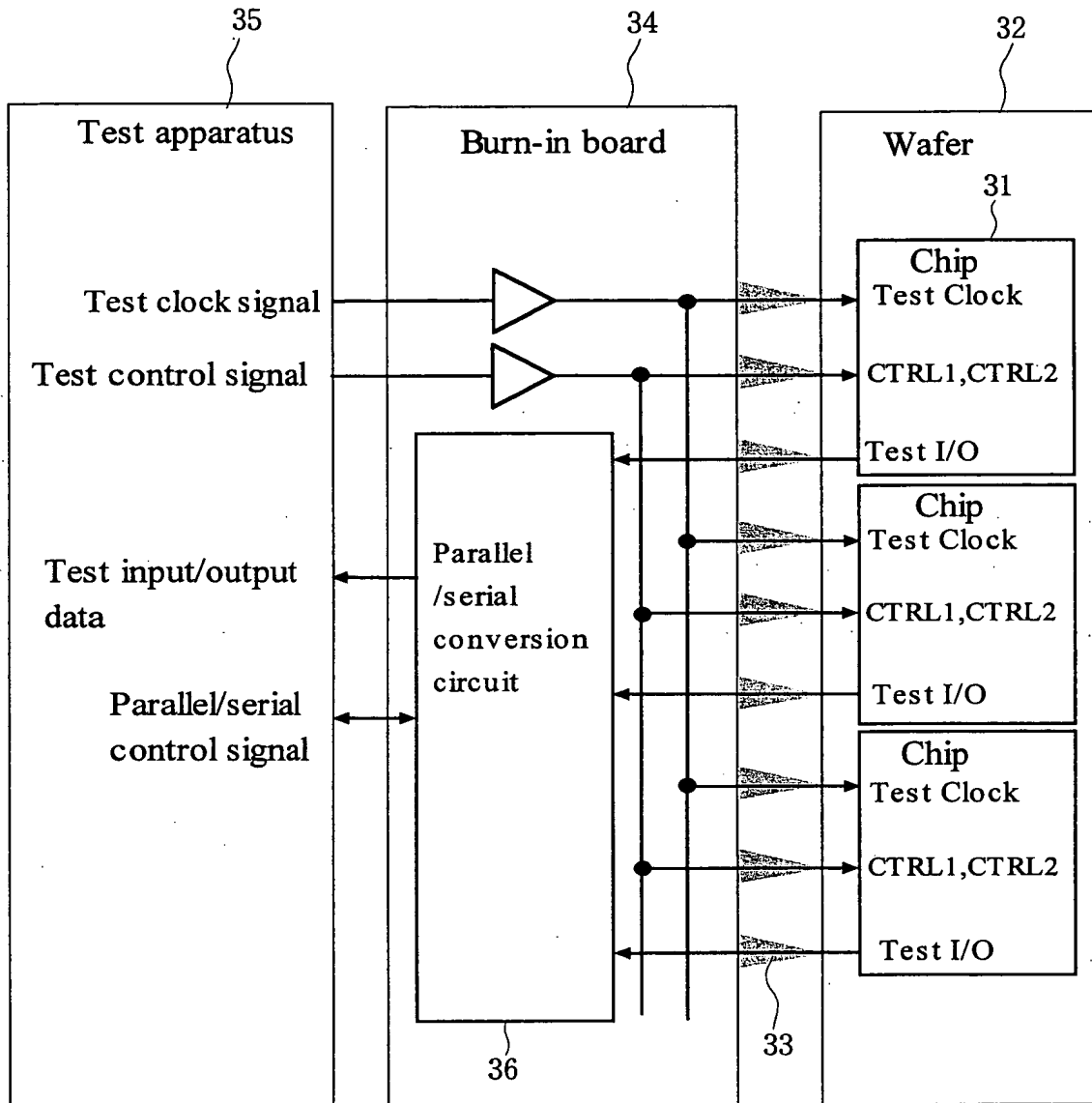
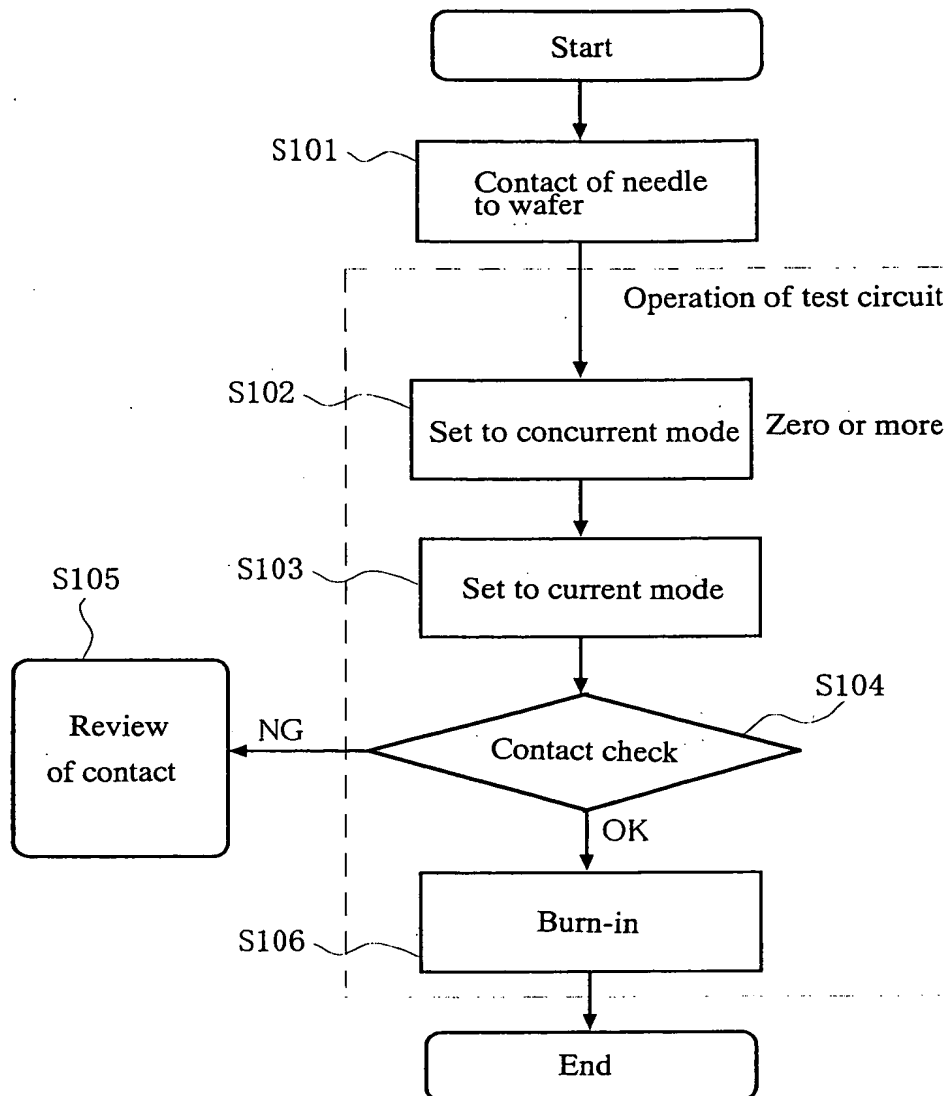


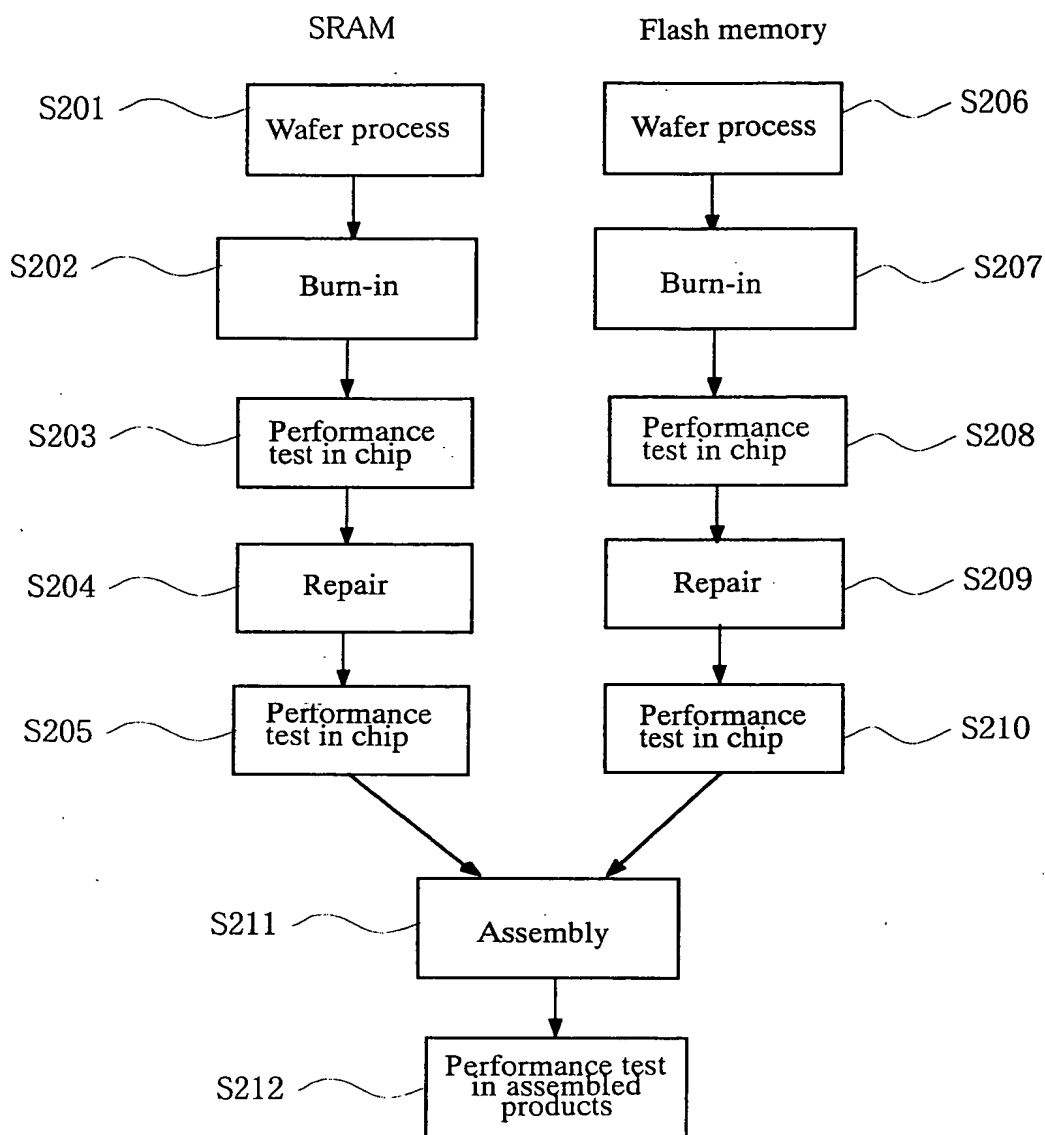
Fig. 6



*Fig. 7*

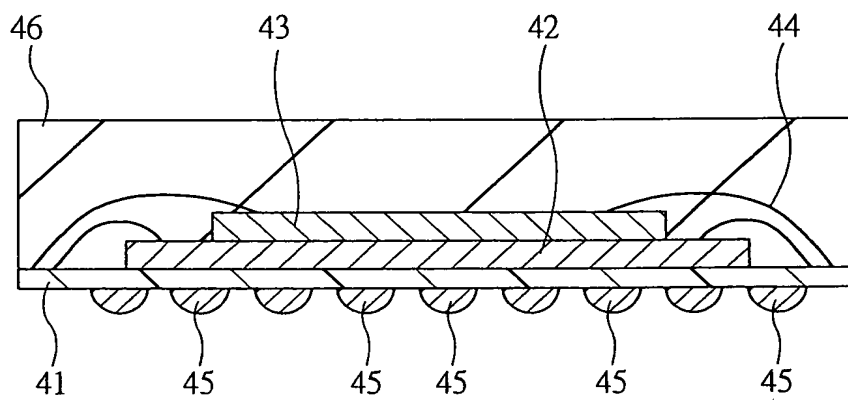


*Fig. 8*

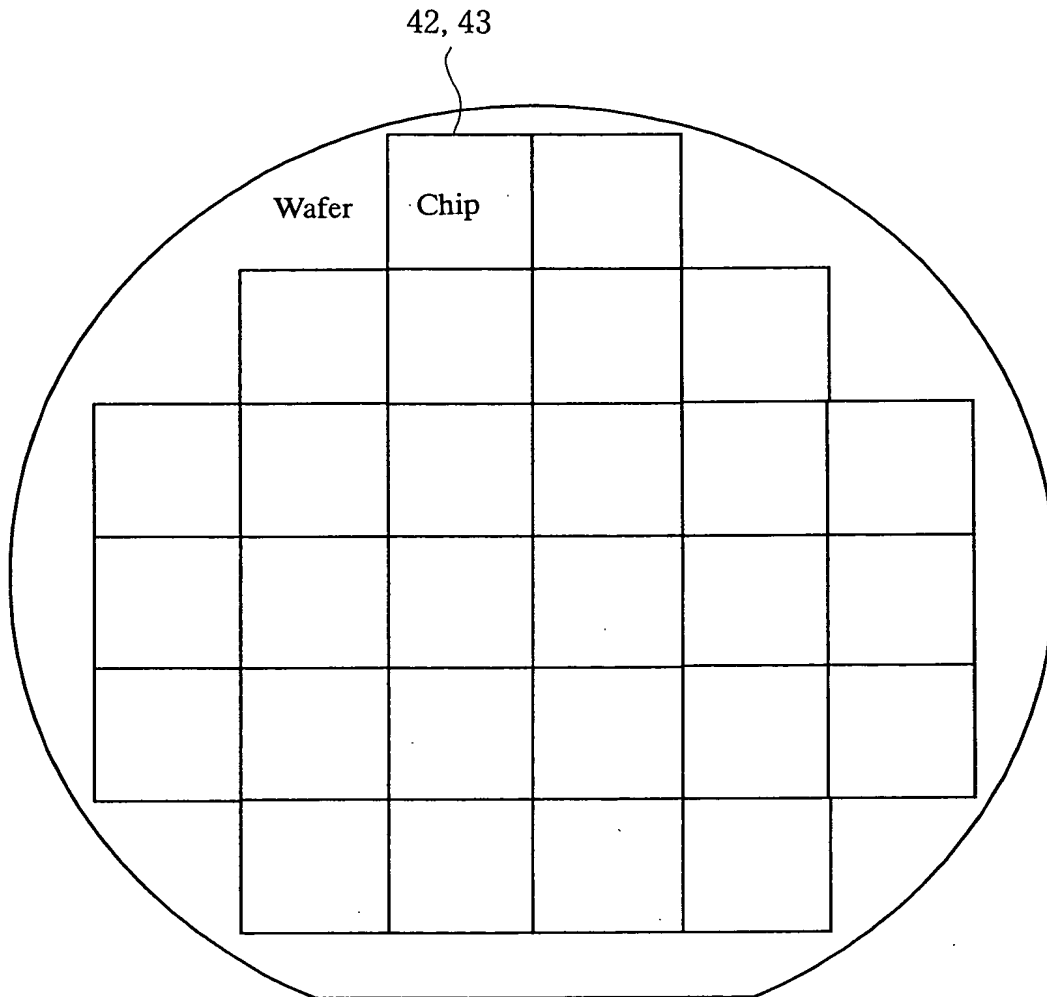




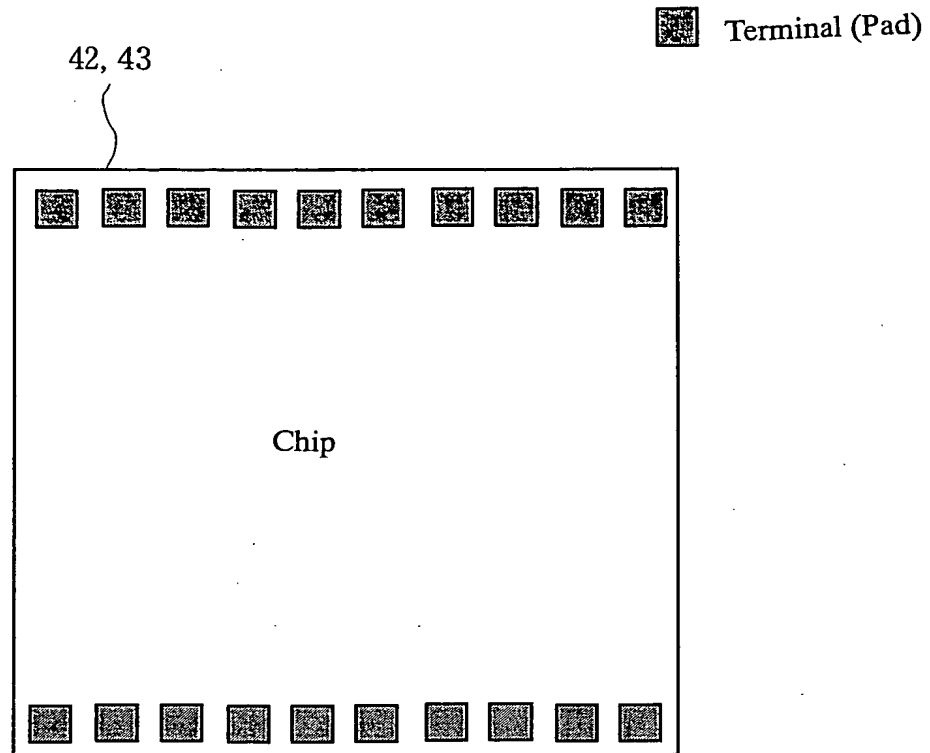
*Fig. 9*



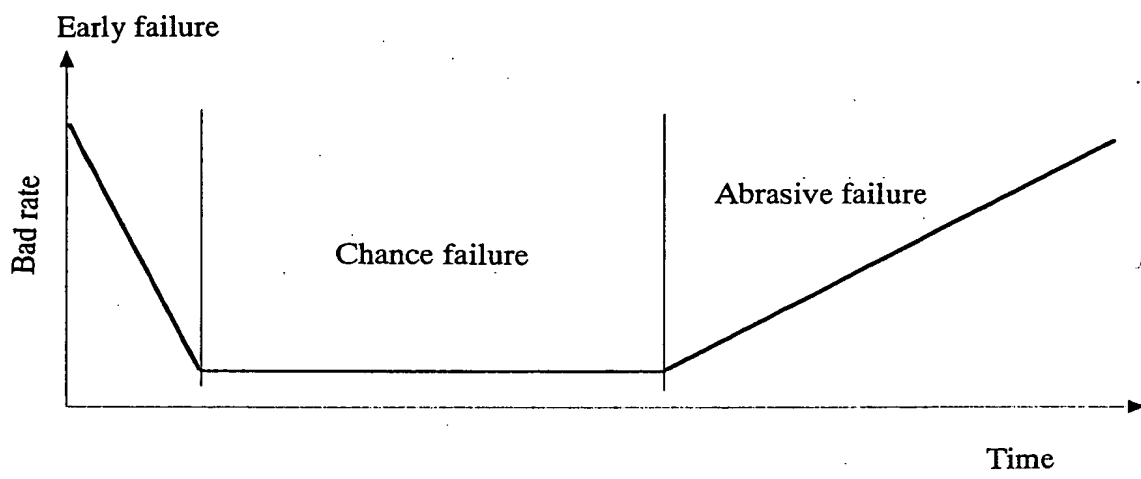
*Fig. 10*



*Fig. 11*



*Fig. 12*



*Fig. 13*

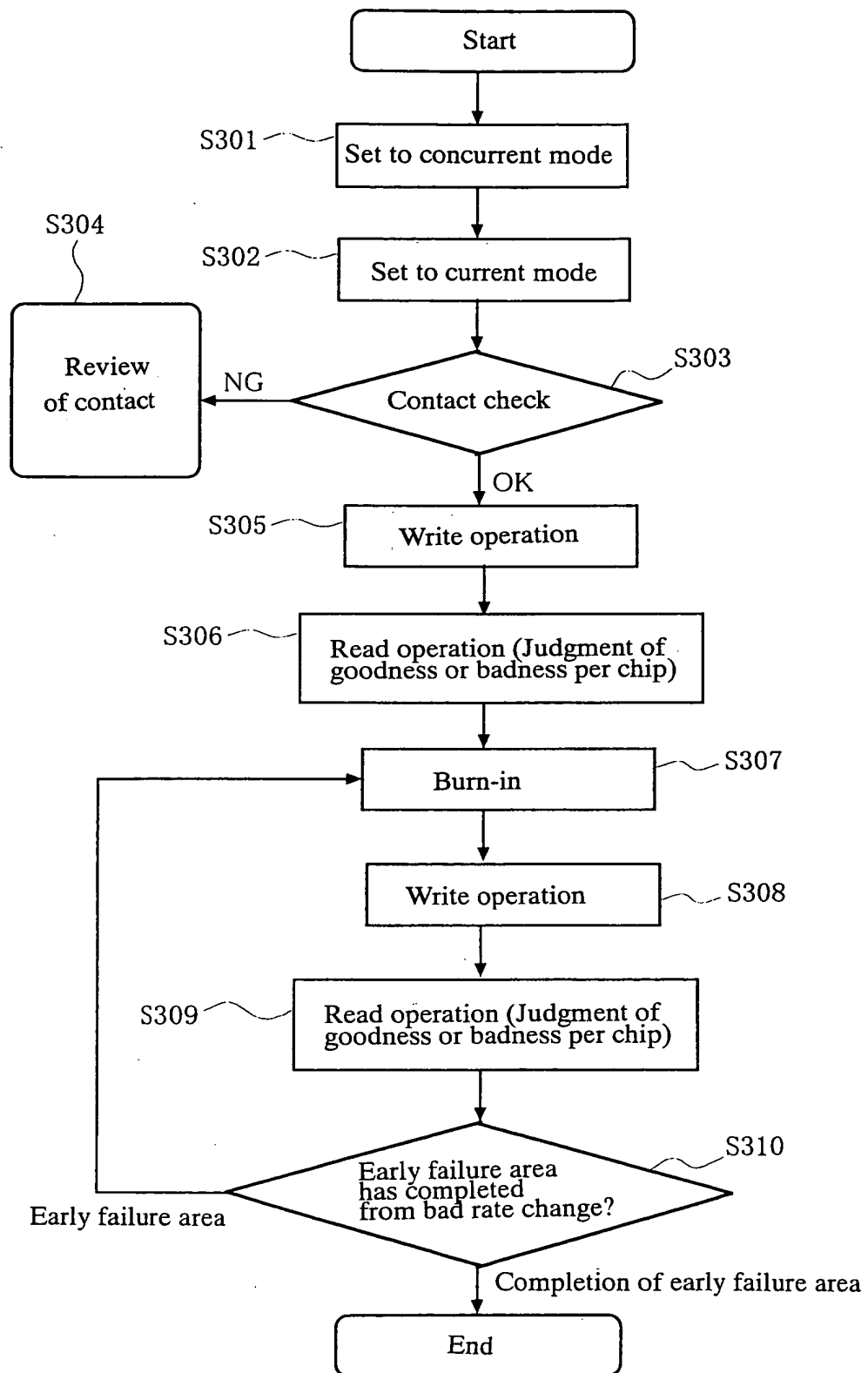


Fig. 14

Operation mode Set timing

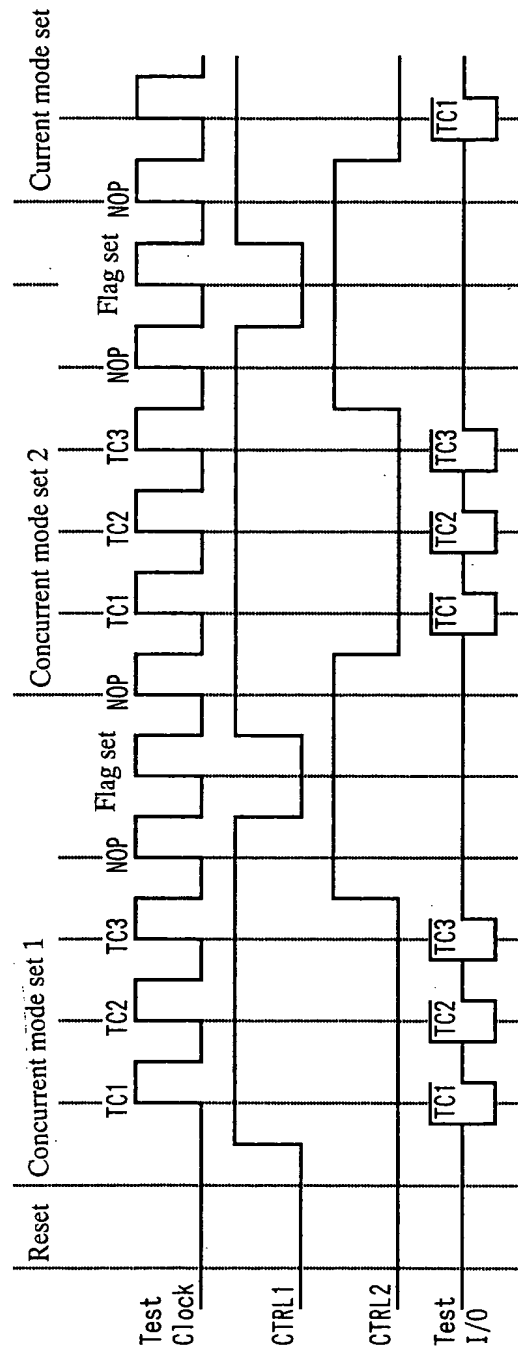


Fig. 15

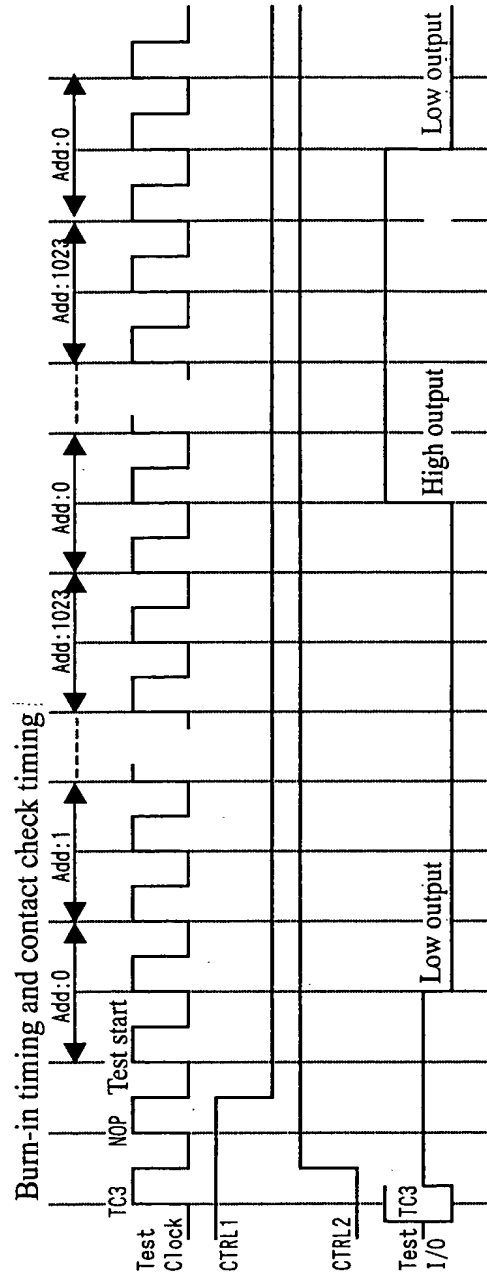
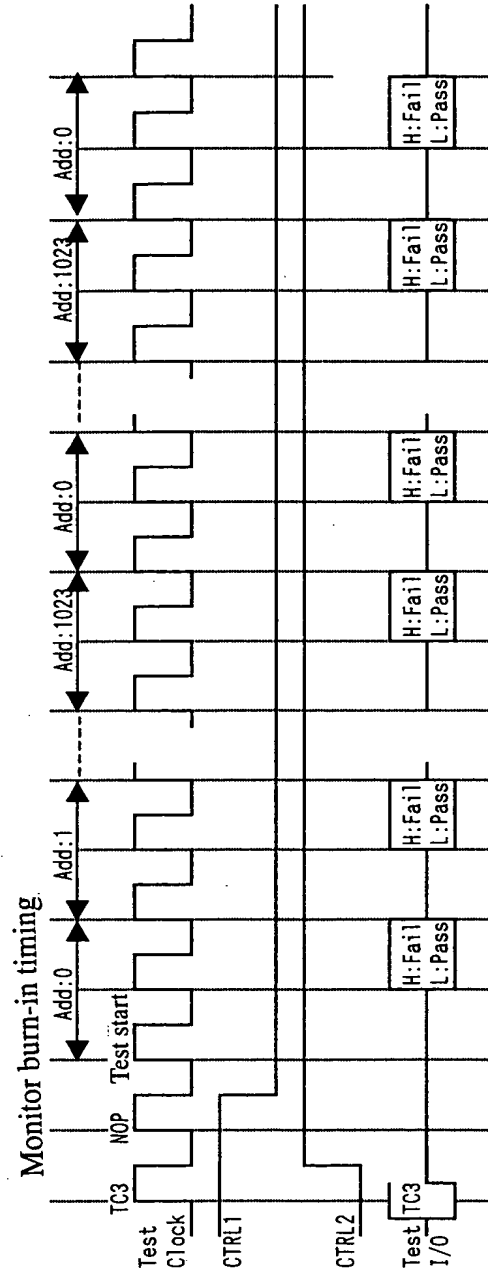


Fig. 16





*Fig. 17*

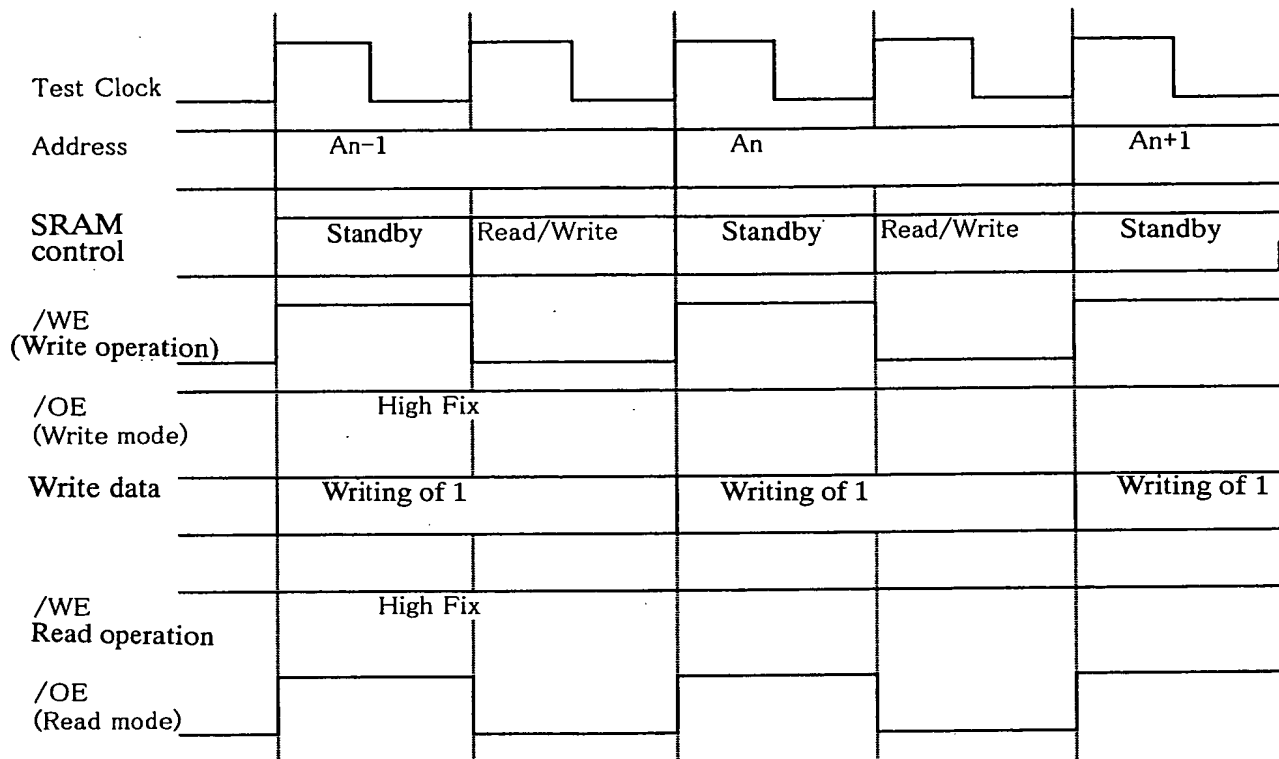
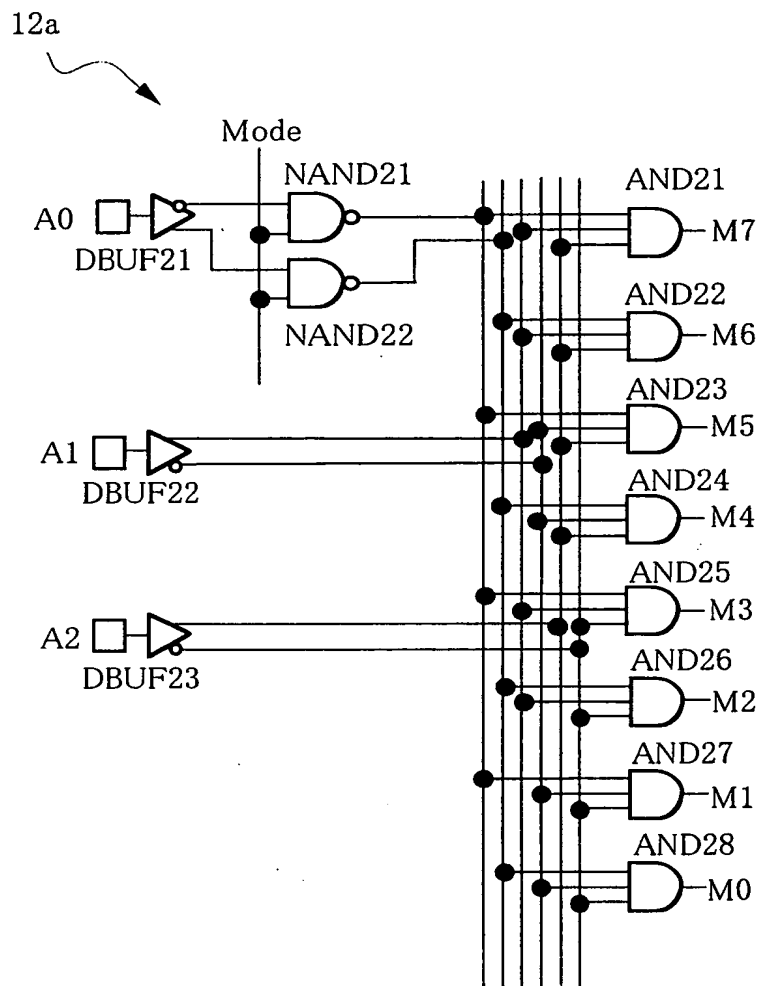


Fig. 18



*Fig. 19*

A0	A1	A2	Mode	M0	M1	M2	M3	M4	M5	M6	M7
0	0	0	1	1	0	0	0	0	0	0	0
1	0	0	1	0	1	0	0	0	0	0	0
0	1	0	1	0	0	1	0	0	0	0	0
1	1	0	1	0	0	0	1	0	0	0	0
0	0	1	1	0	0	0	0	1	0	0	0
1	0	1	1	0	0	0	0	0	1	0	0
0	1	1	1	0	0	0	0	0	0	1	0
1	1	1	1	0	0	0	0	0	0	0	1
0	0	0	0	1	1	0	0	0	0	0	0
1	0	0	0	1	1	0	0	0	0	0	0
0	1	0	0	0	0	1	1	0	0	0	0
1	1	0	0	0	0	1	1	0	0	0	0
0	0	1	0	0	0	0	0	1	1	0	0
1	0	1	0	0	0	0	0	1	1	0	0
0	1	1	0	0	0	0	0	0	0	1	1
1	1	1	0	0	0	0	0	0	0	1	1

Mode=1: Normal decode operation (Always selecting one line)

Mode=0: Multi-choice decode operation (Always selecting two lines)

Fig.20

